Problem Description

To integrate logical left, logical right, arithmetic right shift operations and set less than (SLT) operation for the existing 16-bit ALU (Arithmetic Logic Unit) and register.

Literature survey

Existing Arithmetic Logic Unit and Register

The existing 16-bit ALU had the capability to perform 4 operations on the two 16-bit inputs, which were addition, subtraction, bitwise or and bitwise and. The ALU was further integrated with a 16-bit, 8 word register file. The contents of two registers could be read from the register file at the same time, have an operation be performed on them by the ALU and the result be stored back into a given register. To solve the problem statement four more operations needed to be incorporated to the ALU which are shift-left logically(SLL), shift-right logically(SRL), shift-right arithmetically(SRA), and set less than(SLT). New modules had to be created to do so. They are explained in the following paragraphs.

New modules being incorporated

mux\_16

It is a 1 bit 16:1 mux made using two 8:1 mux and one 2:1 mux from the lib.v file. It takes 16 one bit inputs and pushes one of them as the output based on the 4 bit selection input.

sll

This component takes a sixteen bit input and a 4 bit shamt (shift amount) and shifts the input to the left accordingly by using 16 mux\_16s, appending zeros at the end.

srl

This component takes a sixteen bit input and a 4 bit shamt (shift amount) and shifts the input to the right accordingly by using 16 mux\_16s, appending zeros at the beginning.

sra

This component takes a sixteen bit input and a 4 bit shamt (shift amount) and shifts the input to the right accordingly by using 16 mux\_16s, appending the most significant bit (MSB) at the beginning.

mux8\_16

This component represents a sixteen bit 8:1 mux which is made using eight 8:1 mux from lib.v file. It takes in eight 16-bit inputs and outputs one of them based on 3 bit selection input.

References

* Digital Design and Computer Architecture  [Section 5.2.5, page 250,251]

By David Harris and Sarah L. Harris

* Assignment files for Digital Design and Computer Organization Laboratory, (UE17CS106), PES University.



